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06ES32

Third Semester B.E. Degree Examination, June / July 2014
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the stray capacitance of a diode at high frequency when it is (i) Forward biased and (ii) Reverse biased. **(04 Marks)**

b. In the circuit shown in Fig. Q1 (b) when the input varies linearly from 0 to 150 volts, sketch the output voltage to the time scale assuming the ideal diodes. **(08 Marks)**

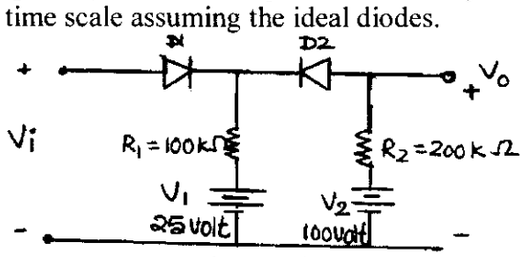

Fig. Q1 (b)

c. Explain the working of circuit shown in Fig. Q1 (c) and also sketch the output waveform. Also calculate the value of resistance R required to have a time constant equal to five times the product of RC during the discharge period. Given $V_r = 0.7$ volt for Si diode. **(08 Marks)**

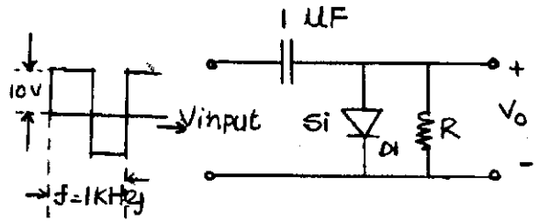

Fig. Q1 (c)

2 a. Find the quiescent collector current I_C and voltage V_{CE} for the circuit shown in Fig. Q2 (a) using exact analysis. Assume $V_{BE} = 0.7$ volt and $B = 80$. **(08 Marks)**

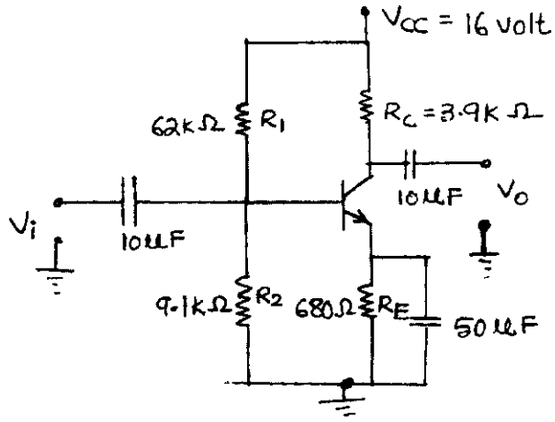

Fig. Q2 (a)

2 b. Derive the expression for the stability factor $S_{(ICO)}$, $S_{(V_{BE})}$ and $S_{(B)}$ for the fixed bias circuit. **(06 Marks)**

c. Determine the value of R_B and R_C for the circuit shown in Fig. Q2 (c). Given V_{BE} = 0.7 volt and I_{Csat} = 20 mA. Select the base current I_B, 50% more to ensure saturation. **(06 Marks)**

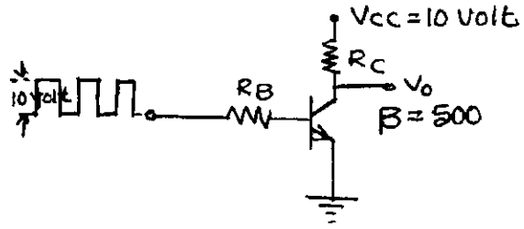

Fig. Q2 (c)

3 a. Find Zi, Zo, Av and A_I for the common base circuit shown in Fig. Q3 (a) using approximate hybrid model. **(10 Marks)**

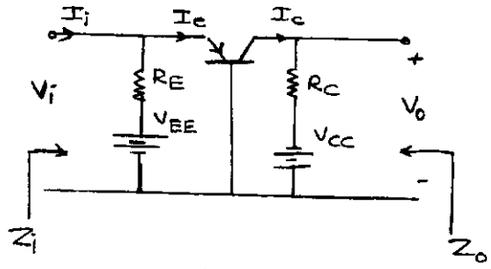

Fig. Q3 (a)

b. For the network shown in Fig. Q3 (b) determine the following parameters using complete hybrid equivalent model:
(i) Z_i and Z_i' (ii) Voltage gain A_V (iii) Current gain A_I (iv) Z_O. **(10 Marks)**

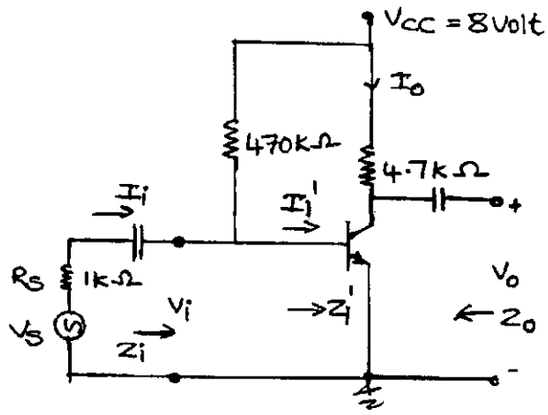

Fig. Q3 (b)

Given h_{fe} = 110, h_{ie} = 1.6 KΩ, h_{re} = 2×10^{-4}, h_{oe} = 20μA/volt

4 a. Describe the Miller effect capacitance and derive an equation for Miller input and output capacitances. **(06 Marks)**

b. Three amplifiers with voltage gain 10, 100 and 1000 are connected in cascade. Find
(i) The overall voltage gain in dB.
(ii) The output voltage when the input voltage is 1 μV. **(04 Marks)**

4 c. Determine the lower cut off frequency f_{LS} for the network shown in Fig. Q4 (c). Given : $V_{CC} = 20$ V, $r_0 = \infty$, B = 100, $R_E = 2$ KΩ, $R_C = 4$ KΩ, $R_L = 2.2$ KΩ. **(10 Marks)**

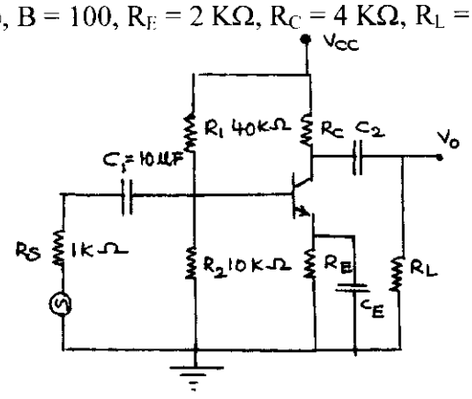

Fig. Q4 (c)

PART – B

5 a. For the two stage cascade amplifier shown in Fig. Q5 (a), determine
(i) The loaded voltage gain of each stage.
(ii) The total gain of the system A_V and A_{VS}.
(iii) The loaded current gain at each stage. **(08 Marks)**

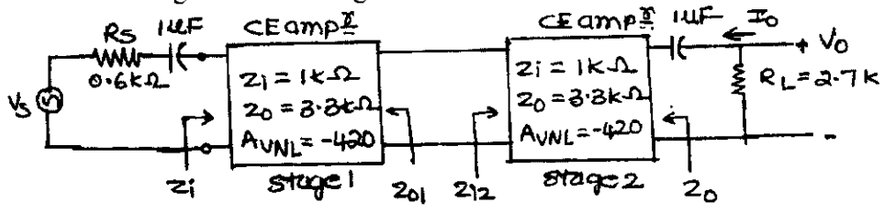

Fig. Q5 (a)

b. Draw the current series feedback circuit and derive an expression to find the output impedance. **(06 Marks)**

c. What is negative feedback and write the advantages of negative feedback? **(06 Marks)**

6 a. Explain the working of a series fed class A power amplifier and also derive an expression to find the max efficiency of the amplifier. **(08 Marks)**

b. A class B push pull amplifier with $V_{CC} = 25$ volt driving a 8 Ω load find,
(i) Maximum input power.
(ii) Maximum output power.
(iii) Maximum circuit efficiency.
(iv) Maximum collector dissipation. **(08 Marks)**

c. What is cross over distortion and how it can be eliminated? **(04 Marks)**

7 a. What is an oscillator? Explain the Bark hausen criterion for sustained oscillations. **(04 Marks)**

b. A quartz crystal has L = 3 Henry, C = 0.05 pf, R = 2 KΩ and $C_M = 10$ pF. Find the series and parallel resonance frequency. **(06 Marks)**

c. Draw the circuit diagram of a Weinbridge oscillator and write the expression to calculate frequency of oscillation and loop gain. **(05 Marks)**

d. In a collpitts oscillator $C_1 = 100$ pF and $C_2 = 60$ pF, find the value of inductor L if the frequency of oscillation required is 50 KHz. **(05 Marks)**

8 a. Draw the ac equivalent for the network shown in Fig. Q8 (a) using small signal ac model and find (i) Input impedence Z_i (ii) Output impedence Z_0 (iii) Voltage gain A_V. **(10 Marks)**

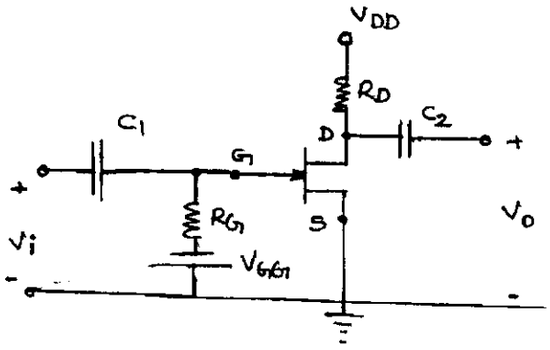

Fig. Q8 (a)

b. For the JFET in common drain configuration shown in Fig. Q8 (b), calculate
(i) The input impedance Z_i.
(ii) Output impedence Z_0.
(iii) Find V_O if V_i = 20 m volt (p – p) **(10 Marks)**

Given : I_{DSS} = 10 mA, V_p = -5 volt, r_d = 40 KΩ, V_{GSQ} = -2.85 volt

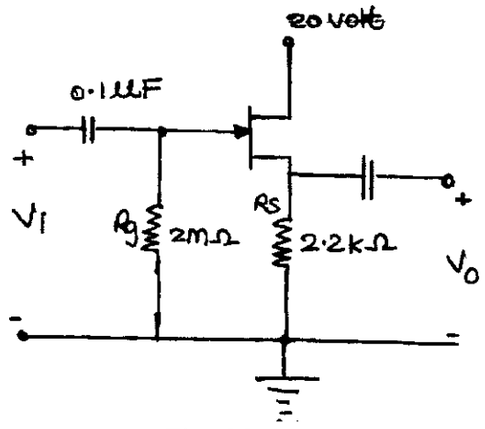

Fig. Q8 (b)

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